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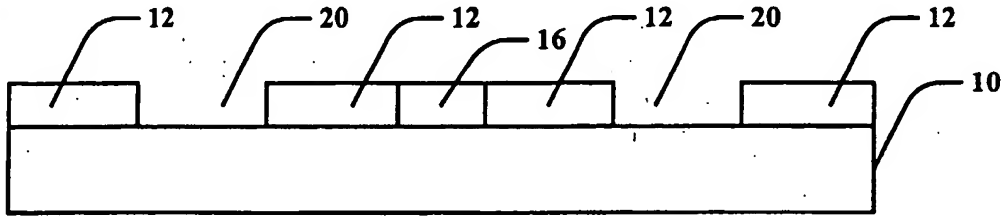
(54) Title: PROCESS FOR MAKING PHOTONIC CRYSTAL CIRCUITS USING AN ELECTRON BEAM AND ULTRAVIOLET LITHOGRAPHY COMBINATION



(57) Abstract: A process for making photonic crystal circuit and a photonic crystal circuit consisting of regularly-distributed holes in a high index dielectric material, and controllably-placed defects within this lattice, creating waveguides, cavities, etc. for photonic devices. The process is based upon the discovery that some positive ultraviolet (UV) photoresists (12) are electron beam sensitive (16) and behave like negative electron beam photoresists. This permits creation of photonic crystal circuits using a combination of electron beam and UV exposures. As a result, the process combines the best features of the two exposure methods: the high speed of UV exposure and the high resolution and control of the electron beam exposure. The process also eliminates the need for expensive photomasks.

WO 03/071587 A1

PROCESS FOR MAKING PHOTONIC CRYSTAL CIRCUITS USING AN ELECTRON BEAM AND ULTRAVIOLET LITHOGRAPHY COMBINATION

CLAIM FOR PRIORITY

The present application claims priority of U.S. Provisional Patent Application Serial No. 60/357,184, filed February 15, 2002, the disclosure of which being incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

A. Field of the Invention

The present invention relates generally to photonic crystals, and, more particularly to a process for making photonic crystal circuits using an electron beam and ultraviolet lithography combination.

B. Description of the Related Art

During the last decade photonic crystals (also known as photonic band gap or PBG materials) have risen from a relatively obscure technology to a prominent field of research. In large part this is due to their unique ability to control, or redirect, the propagation of light. **E. Yablonovich, "Inhibited spontaneous emission in solid-state physics and electronics,"** ***Physical Review Letters*****, vol. 58, pp. 2059-2062 (May 1987),** and **S. John, "Strong localization of photons in certain disordered dielectric superlattices,"** ***Physical Review Letters*****, vol. 58, pp. 2486-2489 (June 1987),** initially proposed the idea that a periodic dielectric structure can possess the property of a band gap for certain frequencies in the electromagnetic spectra, in much the same way as an electronic band gap exists in semiconductor materials. This property affords photonic

crystals with a unique ability to guide and filter light as it propagates within it. In this way, photonic crystals have been used to improve the overall performance of many opto-electronic devices.

The concept of a photonic band gap material is as follows. In direct conceptual analogy to an electronic band gap in a semiconductor material, which excludes electrical carriers having stationary energy states within the band gap, a photonic band gap in a dielectric medium excludes stationary photonic energy states (i.e., electromagnetic radiation having some discrete wavelength or range of wavelengths) within a certain energy range or corresponding frequency range. In semiconductors, the electronic band gap is a consequence of having a periodic atomic structure which interacts with an electron behaving quantum-mechanically as a wave. This interaction gives rise to a forbidden range of energy levels, the so called electronic band gap. By analogy, the photonic band gap results if one has a periodically structured material, where the periodicity is of a distance suitable to interact with an electromagnetic wave of some characteristic wavelength, in such a way as to create a band of frequencies that are forbidden to exist within the material, the so called photonic band gap.

An envisioned use of these materials is the optical analog to semiconductor behavior, in which a photonic band gap material, or a plurality of such materials acting in concert, can be made to interact with and control light wave propagation in a manner analogous to the way that semiconductor materials can be made to interact with and control the flow of electrically charged particles, i.e., electricity, in both analog and digital electronic applications.

Planar photonic crystal circuits such as splitters, high Q-microcavities, and multi-channel drop/add filters have been investigated both theoretically and experimentally in

both two- and three-dimensional photonic crystal structures. For two-dimensional photonic crystal structures, the photonic crystal consists of either an array of low index cylinders surrounded by a background material of sufficiently higher index or, an array of high index cylinders surrounded by a background material of sufficiently lower index. In both cases, in-plane confinement is achieved through multiple Bragg reflections that occur due to the presence of the material lattice, which represents the photonic crystal. For some three-dimensional photonic crystal structures, namely those that consist of a two-dimensional structure, or lattice, that are finite in height, confinement in the vertical direction is achieved through total internal reflection (TIR). In either case the main limiting factor in the wide spread use of these devices is the ability to get light into and out of these structures. For this reason, optical coupling structures have a pronounced impact on the operation of any photonic integrated circuit ("PIC").

In addition, whereas the lithography methods developed in the microelectronic industry have been successfully applied to fabricating small photonic crystal circuits, these methods are far from optimum for this purpose. For example, patterning a square centimeter of photonic crystal circuit for the near infrared wavelength requires exposing approximately 500 million circles. While not impossible, this is certainly strenuous for current lithography tools. Moreover, while slight variation in feature size is acceptable for electronic circuits, the tolerances in case of photonic crystal circuits are far more stringent for even small variation of hole sizes may compromise the performance of photonic crystal circuits.

Thus, there is a need in the art for an improved process for making photonic crystal circuits.

SUMMARY OF THE INVENTION

The present invention addresses the needs of the art by providing a process for making planar photonic crystal circuits consisting of regularly-distributed holes in a high index dielectric material, and controllably-placed defects within this lattice, permitting formation of waveguides, cavities, etc. for creating photonic devices. The process of the present invention is based on the discovery that some positive ultraviolet (UV) photoresists are electron beam ("e-beam") sensitive and behave like negative e-beam photoresists. This permits creation of photonic crystal circuits using a combination of electron beam and UV exposures.

In accordance with the purpose of the invention, as embodied and broadly described herein, the invention comprises a process for making a photonic crystal circuit, comprising: depositing an ultraviolet positive, electron beam negative photoresist layer on a substrate; patterning defects into portions of the photoresist layer by exposing the portions of the photoresist layer to an electron beam; exposing the photoresist layer to ultraviolet radiation; and chemically developing the photoresist layer with a developer, wherein the developer dissolves areas of the photoresist layer exposed to the ultraviolet radiation and unexposed to the electron beam to produce a pattern of holes in the photoresist layer.

Further in accordance with the purpose of the invention, as embodied and broadly described herein, the invention comprises a photonic crystal circuit, comprising: a substrate; and an ultraviolet positive, electron beam negative photoresist layer deposited on the substrate, wherein defects are patterned into portions of the photoresist layer by exposing the portions of the photoresist layer to an electron beam, the photoresist layer is exposed to ultraviolet radiation, and areas of the photoresist layer exposed to the

ultraviolet radiation and unexposed to the electron beam are chemically developed to produce a pattern of holes in the photoresist layer.

Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description. It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

Figs. 1(a)-1(g) are schematic diagrams showing the steps of a process for making a photonic crystal circuit in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and equivalents thereof.

The present invention is drawn to a process for making photonic bandgap (PBG)

structures (or photonic crystal circuits) consisting of regularly-distributed holes in a high index dielectric material, and controllably-placed defects within this lattice, creating waveguides, cavities, etc. for photonic devices. The process of the present invention is based upon the discovery by the present inventors that some positive ultraviolet (UV) photoresists, such as, for example, an AZ 5200 series photoresist sold by Clariant International, Ltd., are electron beam sensitive and behave like negative e-beam photoresists. This permits creation of photonic crystal circuits using a combination of electron beam and UV exposures. As a result, the process of the present invention combines the best features of the two exposure methods: the high speed of UV exposure and the high resolution and control of the electron beam exposure.

Figs. 1(a)-1(g) depict the process of making or patterning a photonic crystal circuit in accordance with an embodiment of the present invention. In a first step of the process, as shown in Figs. 1(a) and 1(b), a UV-positive, e-beam negative photoresist layer 12 may be deposited on a substrate 10 by spinning a liquid solution of the photoresist and then evaporating the solvent of the liquid photoresist solution. Substrate 10 may be a silicon-on-insulator ("SOI"), insulator, silicon, etc. type of substrate. Photoresist layer 12 may comprise any type of UV-positive, e-beam negative type of photoresist, such as, for example, the AZ 5200 series photoresist discussed above.

In a second step of the process of the present invention, defects such as waveguides, cavities, etc., are patterned in photoresist layer 12 using an electron beam 14 as shown in Fig. 1(c). A portion of photoresist layer 12 modified by the e-beam 14 exposure is indicated by reference numeral 16 in Fig. 1(d). However, multiple portions 16 of photoresist layer 12 may be modified by e-beam 14. Electron beam 14 may emanate from any conventional electron beam equipment.

In a third step of the process of the present invention, the structure of Fig. 1(d), i.e., substrate 10, photoresist layer 12, and the e-beam modified portion 16 of photoresist layer 14, is exposed with an interference pattern from coherent sources of ultraviolet radiation 18, as shown in Fig. 1(e). For example, three coherent sources of ultraviolet radiation 18 can create a triangular lattice of bright spots, or antinodes of the interference pattern, in photoresist layer 12. Ultraviolet radiation 18 may emanate from any conventional coherent ultraviolet radiation source.

In the last step of the process of the present invention, photoresist layer 12 is chemically developed with a developer, as shown in Fig. 1(f). The developer may be any conventional type of developer used to develop the specific photoresist chosen for photoresist layer 12 such as, for example, a Microposit 327 MIF developer. The developer dissolves areas of photoresist layer 12 that were exposed to ultraviolet radiation 18 (i.e., bright spots or antinodes of the interference pattern) and unexposed to electron beam 14. Areas of photoresist layer 14 unexposed to ultraviolet radiation 18 or exposed to electron beam 14 remain intact, as shown in Fig. 1(f). This produces a pattern or a regular grid of holes 20 corresponding to the antinodes of the interference patterns produced by ultraviolet radiation 18 and unexposed to electron beam 14.

The pattern of holes 20 in photoresist layer 14 may then be transferred to the underlying substrate 10 using standard etching techniques. Alternatively, a metal layer 22 may be formed under photoresist layer 12 in the case of mask-making. In which case, the pattern of holes 20 would be extended through metal layer 22 using standard metal etching techniques, as shown in Fig. 1(g).

The process of the present invention provides several advantages over conventional techniques since it exploits the best features of UV and electron beam

lithography. UV lithography is suitable for large area fast exposure. Moreover, by using an interference pattern in the UV exposure, the process of the present invention eliminates the use of photomasks, which provides major cost savings since photomasks are expensive to manufacture. The electron beam exposure allows for very high resolution patterning, but is not suitable for a large area since it is a serial, and thus relatively slow, process. However, in the process of the present invention the electron beam is used only to expose specific defects within the structure. Thus, the patterning time is significantly reduced as compared to what would be required had the entire structure been exposed to an electron beam.

It will be apparent to those skilled in the art that various modifications and variations can be made in the process for making photonic crystal circuits using an electron beam and ultraviolet lithography combination of the present invention and in construction of the process without departing from the scope or spirit of the invention. As an example, the primary application of the process of the present invention is the fabrication of photonic crystal-based circuits. However, the process of the present invention could also be used for patterning electronic circuits containing repeatable cells in addition to non-repeatable structures, such as, for example, computer memory or programmable gate arrays. In this case, the repeatable structures would be patterned with the interference pattern of the UV beams, possibly involving numerous coherent beams, whereas the unique patterns would be written with the e-beam. Furthermore, the process of the present invention may also be used to pattern a photolithography mask rather than for direct exposure, thereby greatly reducing the cost of mask making.

Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It

is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

WHAT IS CLAIMED IS:

1. A process for making a photonic crystal circuit, comprising:

depositing an ultraviolet positive, electron beam negative photoresist layer on a substrate;

patterning defects into portions of the photoresist layer by exposing the portions of the photoresist layer to an electron beam;

exposing the photoresist layer to ultraviolet radiation; and

chemically developing the photoresist layer with a developer, wherein the developer dissolves areas of the photoresist layer exposed to the ultraviolet radiation and unexposed to the electron beam to produce a pattern of holes in the photoresist layer.

2. A process for making a photonic crystal circuit as recited in claim 1, wherein the substrate comprises a silicon-on-insulator substrate.

3. A process for making a photonic crystal circuit as recited in claim 1, wherein the depositing of the photoresist layer comprises spinning a liquid solution of the photoresist on the substrate and evaporating a solvent from the liquid solution.

4. A process for making a photonic crystal circuit as recited in claim 1, wherein the photoresist layer comprises an AZ 5200 series photoresist.

5. A process for making a photonic crystal circuit as recited in claim 1, wherein the ultraviolet radiation comprises an interference pattern from coherent sources of ultraviolet radiation.

6. A process for making a photonic crystal circuit as recited in claim 5, wherein three coherent sources of ultraviolet radiation are used to create a triangular lattice of antinodes of the interference pattern in the photoresist layer.

7. A process for making a photonic crystal circuit as recited in claim 6, wherein the pattern of holes correspond to the antinodes of the interference pattern formed in the photoresist layer and the areas of the photoresist layer unexposed to the electron beam.

8. A process for making a photonic crystal circuit as recited in claim 1, wherein the developer comprises a Microposit 327 MIF developer.

9. A process for making a photonic crystal circuit as recited in claim 1, further comprising transferring the pattern of holes to the substrate by etching the substrate.

10. A process for making a photonic crystal circuit as recited in claim 1, further comprising, prior to the depositing the photoresist layer, depositing a metal layer on the substrate.

11. A process for making a photonic crystal circuit as recited in claim 10, further comprising transferring the pattern of holes to the metal layer by etching the metal layer.

12. A photonic crystal circuit, comprising:

a substrate; and

an ultraviolet positive, electron beam negative photoresist layer deposited on the substrate, wherein defects are patterned into portions of the photoresist layer by exposing the portions of the photoresist layer to an electron beam, the photoresist layer is exposed to ultraviolet radiation, and areas of the photoresist layer exposed to the ultraviolet radiation and unexposed to the electron beam are chemically developed to produce a pattern of holes in the photoresist layer.

13. A photonic crystal circuit as recited in claim 12, wherein the substrate comprises a silicon-on-insulator substrate.

14. A photonic crystal circuit as recited in claim 12, wherein the photoresist layer comprises an AZ 5200 series photoresist.

15. A photonic crystal circuit as recited in claim 12, wherein a triangular lattice of antinodes of an interference pattern are created in the photoresist layer with the ultraviolet radiation.

16. A photonic crystal circuit as recited in claim 15, wherein the pattern of holes correspond to the antinodes of the interference pattern formed in the photoresist layer and the areas of the photoresist layer unexposed to the electron beam.

17. A photonic crystal circuit as recited in claim 12, wherein the developer comprises a Microposit 327 MIF developer.

18. A photonic crystal circuit as recited in claim 12, wherein the pattern of holes is transferred to the substrate by etching the substrate.

19. A photonic crystal circuit as recited in claim 12, further comprising a metal layer deposited on the substrate below the photoresist layer.

20. A photonic crystal circuit as recited in claim 19, wherein the pattern of holes is transferred to the metal layer by etching the metal layer.

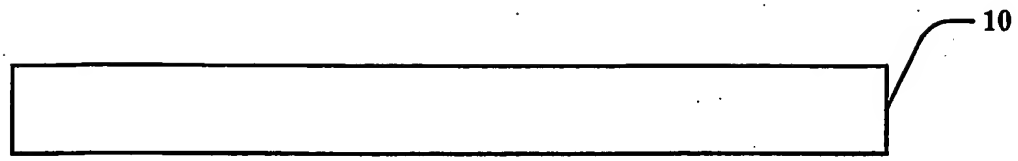


Fig. 1(a)

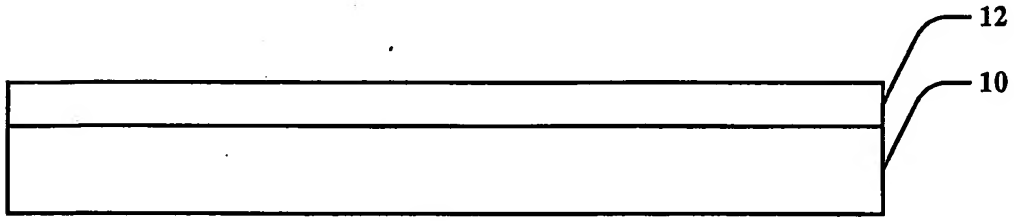


Fig. 1(b)

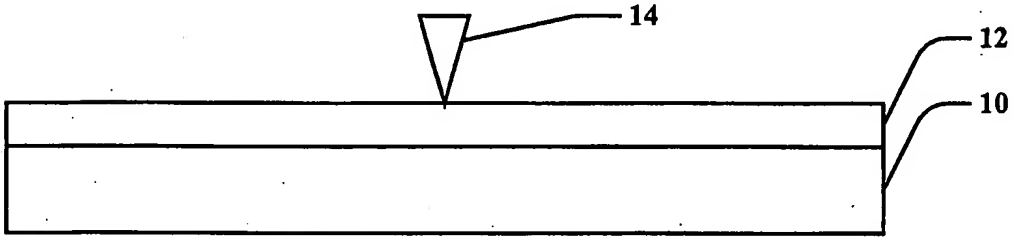


Fig. 1(c)

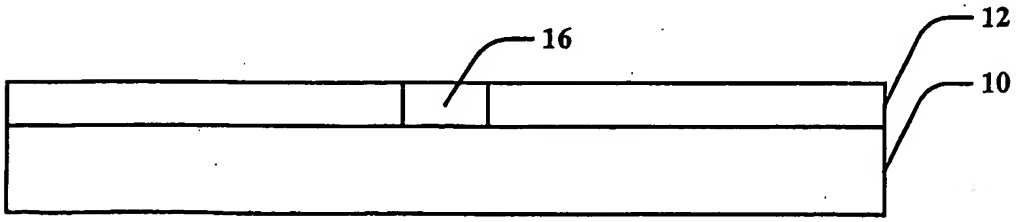


Fig. 1(d)

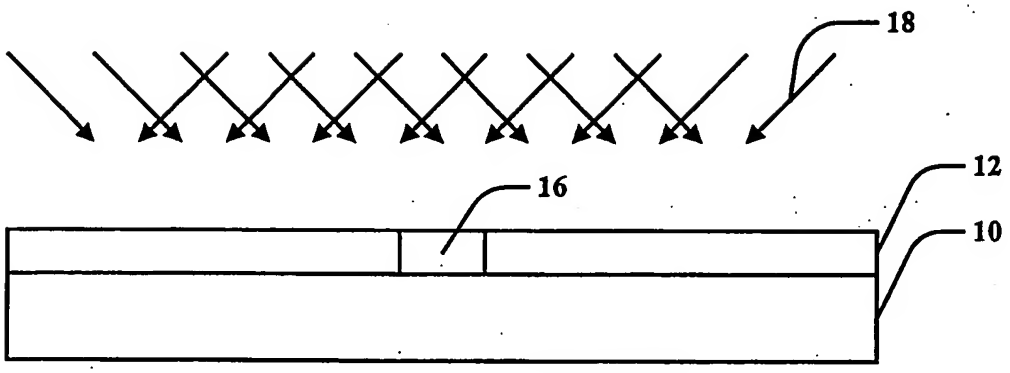


Fig. 1(e)

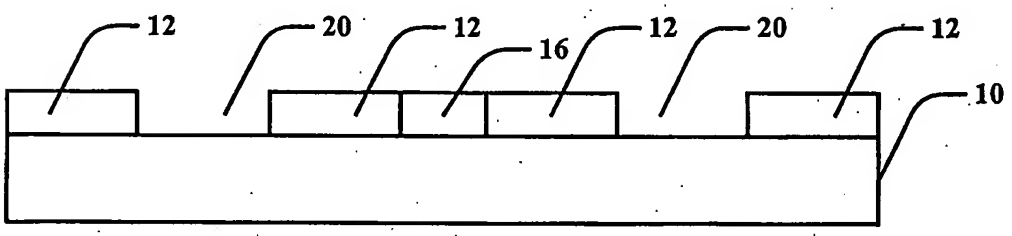


Fig. 1(f)

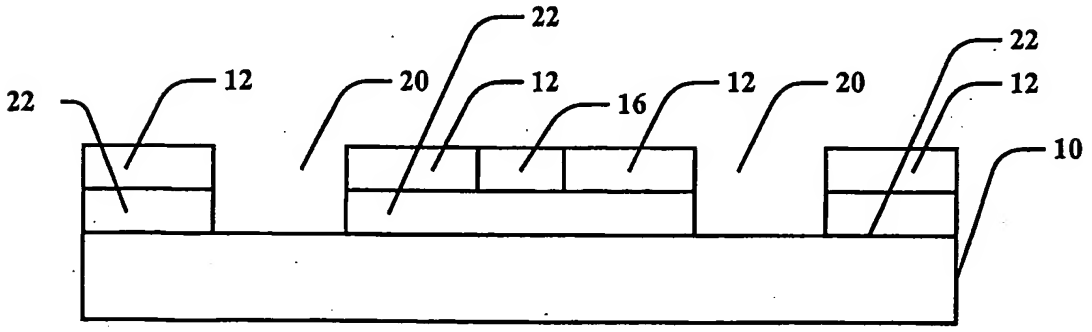


Fig. 1(g)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/04682

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/00
US CL : 438/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 216/41, 49, 66; 430/5, 296; 438/707, 708, 725

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
East

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,328,560 A (HANAWA ET AL) 12 July 1994 (12/07/94), see entire document.	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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